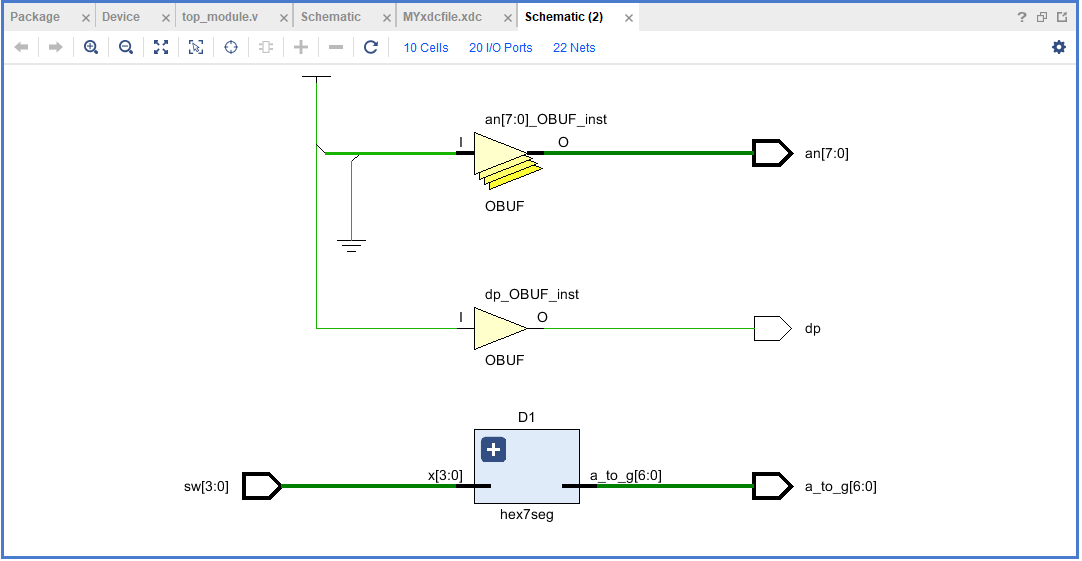
**IMPLEMENTATION/INTERFACING OF SEVEN SEGMENT DISPLAY ON FPGA (NEXYS 4) BOARD.**

**SCHEMATIC**

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**Verilog/source code**

module top\_module(

input wire [3:0] sw,

output wire [6:0] a\_to\_g,

output wire [7:0] an,

output wire dp

);

assign an = 8'b11111110;

assign dp = 1;

hex7seg D1(.x(sw), .a\_to\_g(a\_to\_g));

endmodule

//////////////////////////////////////////////////////////////////////////////////

//////////////////////////////////////////////////////////////////////////////////

module hex7seg(

input wire [3:0]x,

output reg [6:0]a\_to\_g

);

always@(\*)

begin

case(x)

0: a\_to\_g = 7'b0000001;

1: a\_to\_g = 7'b1001111;

2: a\_to\_g = 7'b0010010;

3: a\_to\_g = 7'b0000110;

4: a\_to\_g = 7'b1001100;

5: a\_to\_g = 7'b0100100;

6: a\_to\_g = 7'b0100000;

7: a\_to\_g = 7'b0001111;

8: a\_to\_g = 7'b0000000;

9: a\_to\_g = 7'b0000100;

'hA: a\_to\_g= 7'b0001000;

'hB: a\_to\_g= 7'b1100000;

'hC: a\_to\_g= 7'b0110001;

'hD: a\_to\_g= 7'b1000010;

'hE: a\_to\_g= 7'b0110000;

'hF: a\_to\_g= 7'b0111000;

default: a\_to\_g = 7'b0000001;

endcase

end

endmodule

**MYxdcfile.xdc**

set\_property IOSTANDARD LVCMOS33 [get\_ports {a\_to\_g[6]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {a\_to\_g[5]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {a\_to\_g[4]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {a\_to\_g[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {a\_to\_g[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {a\_to\_g[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {a\_to\_g[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an[7]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an[6]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an[5]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an[4]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports dp]

set\_property PACKAGE\_PIN U9 [get\_ports {sw[0]}]

set\_property PACKAGE\_PIN R7 [get\_ports {sw[2]}]

set\_property PACKAGE\_PIN R6 [get\_ports {sw[3]}]

set\_property PACKAGE\_PIN U8 [get\_ports {sw[1]}]

set\_property PACKAGE\_PIN M4 [get\_ports dp]

set\_property PACKAGE\_PIN L3 [get\_ports {a\_to\_g[6]}]

set\_property PACKAGE\_PIN N1 [get\_ports {a\_to\_g[5]}]

set\_property PACKAGE\_PIN L5 [get\_ports {a\_to\_g[4]}]

set\_property PACKAGE\_PIN L4 [get\_ports {a\_to\_g[3]}]

set\_property PACKAGE\_PIN K3 [get\_ports {a\_to\_g[2]}]

set\_property PACKAGE\_PIN M2 [get\_ports {a\_to\_g[1]}]

set\_property PACKAGE\_PIN L6 [get\_ports {a\_to\_g[0]}]

set\_property PACKAGE\_PIN N6 [get\_ports {an[0]}]

set\_property PACKAGE\_PIN M6 [get\_ports {an[1]}]

set\_property PACKAGE\_PIN M3 [get\_ports {an[2]}]

set\_property PACKAGE\_PIN N5 [get\_ports {an[3]}]

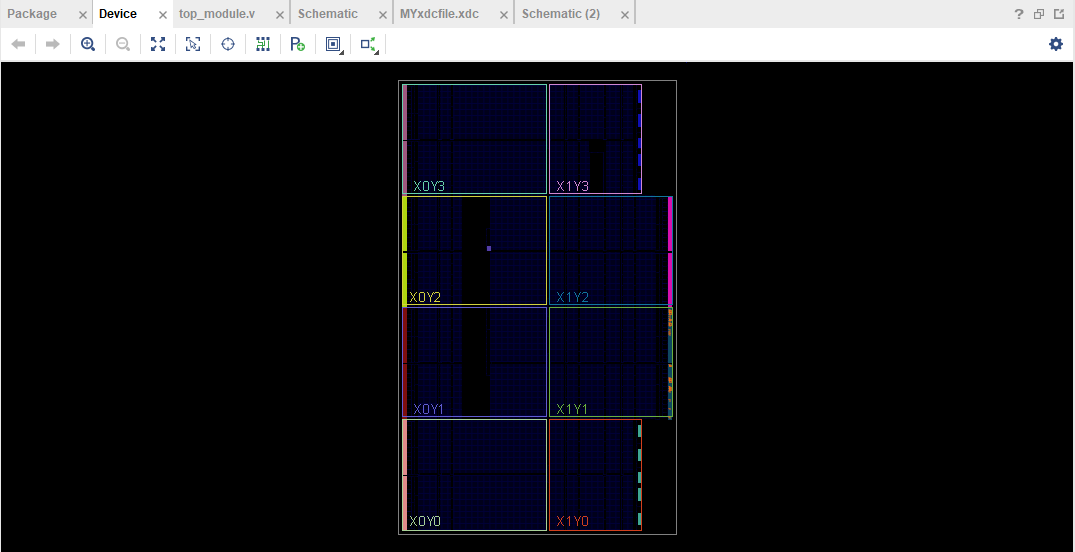
set\_property PACKAGE\_PIN N2 [get\_ports {an[4]}]

set\_property PACKAGE\_PIN N4 [get\_ports {an[5]}]

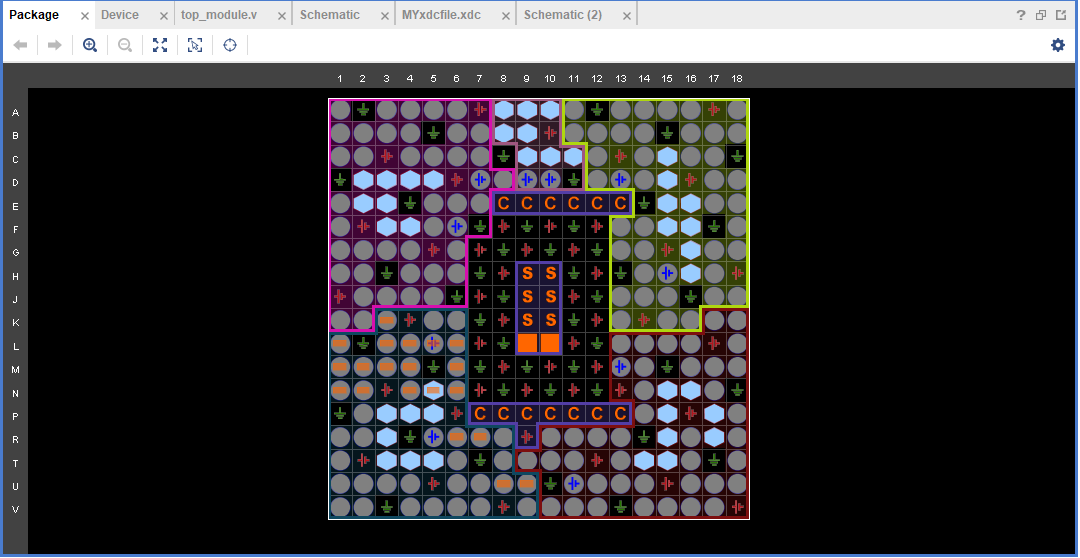
set\_property PACKAGE\_PIN L1 [get\_ports {an[6]}]

set\_property PACKAGE\_PIN M1 [get\_ports {an[7]}]

**DEVICE**

****

**PACKAGE**

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**FPGA BOARD (NEXYS 4)**

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**General Purpose I/O devices on the Nexys 4**

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